IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Hsiao, Chia-Shun		
Assignee:	Mosel Vitelic, Inc.		
Title:	Floating Gate Memory Structures And Fabrication Methods		
Application No.:	Unknown	Filing Date:	Herewith
Examiner:	Unknown	Group Art Unit:	Unknown
Docket No.:	M-12200-1D US		

San Jose, California
September 9, 2003

Mail Stop Patent Application
Director of the USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are not enclosed as all documents were previously cited by or submitted to the Patent Office in prior applications relied upon for priority under 35 U.S.C. 120(37 C.F.R. § 1.98(d)). The prior applications are U.S. Application No. 10/266,378, filed October 7, 2002.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be material to patentability as defined in § 1.56(b).

EXPRESS MAIL LABEL NO.:

EV 301 054 476 US

Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-12200-1D US	Unassigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Chia-Shun Hsiao	
	Filing Date	Group
	Herewith	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,940,717	17 Aug. 1999	Rengarajan et al.			
	AB	6,127,215	3 Oct. 2000	Joachim et al			
	AC	6,130,129	10 Oct. 2000	Chen			
	AD	6,200,856 B1	13 Mar. 2001	Chen			
	AE	6,319,794 B1	20 Nov. 2001	Akatsu et al.			
	AE	6,355,524	12 Mar. 2002	Tuan et al.			
	AG	6,518,618	11 Feb. 2003	Fazio et al.			
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AO	Aritome, S. et al. "A 0.67um^2 Self-Aligned Shallow Trench Isolation Cell (SA-STI Cell For 3V-only 256Mbit NAND EEPROMs," International Electron Devices meeting 1994, San Francisco, CA December 11-14, 1994, pages 94-61 – 94-64.
	AP	Keeney, Stephen N., "A 130nm Generation High Density Etox TM Flash Memory Technology, Intel, Corporation, Santa Clara, CA USA 42 Sheets.
	AQ	Silicon, Flash and Other Non-Volatile Memory Technologies, http://www.inttel.com/research/silicon/flash.htm, September 12, 2002, pages 1-4.
	AR	United States Patent Application No. 10/262,785, entitled "Floating Gate Memory Fabrication Methods Comprising A Field Dielectric Etch With A Horizontal Etch Component," filed on October 1, 2002, Inventor: Yi Ding, Attorney Docket No.: M-12841 US.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.